CLAIMS

We claim:

1. A memory cell comprising:

a steering element for providing enhanced current flow in one direction through the steering element;

a state change element for retaining a programmed state, connected in series with the steering element such that the steering element and state change element provide a two terminal cell;

the steering element and state change element being vertically aligned with one another.

2. The cell defined by claim 1 wherein the steering element is fabricated from polysilicon.

3. The cell defined by claim 2 wherein the polysilicon is doped so as to form a diode.

4. The cell defined by claim 1 wherein the steering element is a metal-semiconductor Schottky diode.

5. The cell defined by claim 1 wherein the steering element is a junction field-effect transistor with a gate connected to one of a source or drain region.

6. The cell defined by claim 1 wherein the steering element is a field-effect transistor having an insulated gate connected to one of a source or drain regions.

7. The cell defined by claim 1 wherein the steering element is a PN junction diode formed in amorphous semiconductor.

8. The cell defined by claim 1 wherein the steering element is a Zener diode.

9. The cell defined by claim 1 wherein the steering element is an avalanche diode.

10. The cell defined by claim 1 wherein the steering element is a tunnel diode.

11. The cell defined by claim 1 wherein the steering element is a four -layer diode (SCR).

12. The cell defined by claim 1 wherein the state change element is an antifuse.

13. The cell defined by claim 12 wherein the antifuse is formed from polysilicon.

14. The cell defined by claim 12 wherein the antifuse includes silicon dioxide.

15. The cell defined by claim 1 wherein the state change element is a dielectric-rupture antifuse.

16. The cell defined by claim 1 wherein the state change element is a polycrystalline semiconductor antifuse.

17. The cell defined by claim 1 wherein the state change element is an amorphous semiconductor antifuse.

18. The cell defined by claim 1 wherein the state change element is a metal filament electromigration fuse.

19. The cell defined by claim 1 wherein the state change element is a polysilicon resistor-fuse.

20. The cell defined by claim 1 wherein the state change element employs trap-induced hysteresis.

21. The cell defined by claim 1 wherein the state change element employs a ferroelectric capacitor.

22. The cell defined by claim 1 wherein the state change element employs a Hall effect device.

23. The cell defined by claim 1 wherein the steering element comprises a diode and the state change element comprises an antifuse, and where the diode is able to carry a sufficient current to change the state of the antifuse.

24. The cell defined by claim 1 wherein the steering element comprises a recrystallized semiconductor.

25. The cell defined by claim 1 wherein the steering element and state change element include amorphous silicon.

26. The cell defined by claim 1 wherein one of the terminals of the cell is connected to a word line.

27. The cell defined by claim 26 wherein the other of the terminals of the cell is connected to a bit line.

28. A memory cell comprising:

a pillar having a generally rectangular cross-section and having at one end a steering element which more readily conducts current in one direction, and a state change element located at the other end of the pillar , the state change element for recording a state.

29. The memory cell defined by claim 28 wherein the steering element comprises a diode.

30. The memory cell defined by claim 29 wherein the diode comprises polysilicon.

31. The memory cell defined by claim 28 wherein the state change element comprises a , dielectric rupture antifuse.

32. The memory cell defined by claim 31 wherein the antifuse comprises a silicon dioxide layer sandwiched between two layers of polysilicon.

33. The memory cell defined by claim 28 having a first conductor in contact with the steering element, the first conductor having a width approximately equal to one dimension of the rectangular cross-section.

34. The memory cell defined by claim 33 having a second conductor in contact with the state change element, the second conductor having a width approximately equal to the other dimension of the rectangular cross-section.

35. A memory array comprising:

a first plurality of spaced-apart, parallel, substantially coplanar conductors;

a second plurality of spaced-apart, parallel, substantially coplanar conductors disposed generally vertically above and spaced-apart from the first conductors, said first and second conductors being generally orthogonal to one another; and

a plurality of first memory cells, each cell disposed between one of the first and one of the second conductors and located where a vertical projection of the first conductors intersects the second conductors, the cells being vertically aligned with at least one of the conductors.

36. The array defined by claim 35 wherein the cells are aligned with both the first and second conductors.

37. The array defined by claim 35 wherein the cells each comprise a steering element and a state change element.

38. A memory array comprising:

a first plurality of spaced-apart, parallel, substantially coplanar conductors;

a second plurality of spaced-apart, parallel, substantially coplanar conductors disposed generally vertically above and spaced-apart from the first conductors, said first and second conductors being generally orthogonal to one another; and

a plurality of first memory cells, each cell disposed between one of the first and one of the second conductors and located where a vertical projection of the first conductors intersects the second conductors;

a third plurality of spaced-apart, parallel, substantially coplanar conductors disposed generally vertically above and spaced-apart from the second conductors, the third conductors running in the same direction as the first conductors;

a plurality of second memory cells, each cell disposed between one of the second conductors and one of the third conductors and located where a vertical projection of the second conductors intersects the third conductors.

39. The array defined by claim 38 wherein first cells and second cells are in vertical alignment with one another.

40. The array defined by claim 38 wherein the first cells and second cells are staggered from one another.

41. The array defined by claim 38 wherein each of the first cells and the second cells comprise a steering element and a state change element.

42. The array defined by claim 41 wherein the steering elements of the first and second cells are connected to the second conductors.

43. The array defined by claim 41 wherein the state change elements of the first and second cells are connected to the second conductors.

44. The array defined by claim 38 wherein the first and second cells have a generally rectangular cross-section.

45. The array defined by claim 38 wherein the first and second cells comprise polysilicon and silicon dioxide.

46. The array defined by claim 38 wherein the first and second cells comprise polysilicon.

47. The array defined by claim 38 wherein the array is fabricated on a silicon substrate.

48. The array defined by claim 47 includes a first contact extending from one of the second conductors to a first region in the substrate.

49. The array defined by claim 48 including a second contact extending from one of the first conductors to a second region in the substrate.

50. The array defined by claim 38 wherein the first and second conductors include a refractory metal.

51. The array defined by claim 50wherein the refractory metal is tungsten.

52. The array defined by claim 38 wherein the first and second conductors are a silicide.

53. A memory array comprising:

a plurality of conductors on levels 1, 2, 3, 4... where the levels are parallel and spaced-apart, the conductors in the odd numbered levels 1, 3... running in a first direction,

the levels in the even numbered levels 2, 4... running in a second direction, generally perpendicular to first direction, and

a plurality of memory cells each having an input terminal and an output terminal, the cells being disposed between conductors in each of the levels 1, 2, 3, 4... .

54. The array defined by claim 53 wherein the input terminals of the cells are connected to the conductors in the odd numbered levels 1, 3... and the output terminals of the cells are connected to the conductors in the even numbered levels 2, 4... .

55. The array defined by claim 53 wherein the output terminal of the cells are connected to the conductors in the odd numbered levels 1, 3... and the input terminal of the cells are connected to the conductors in the even numbered levels 2, 4... .

56. The array defined by claims 54 or 55 wherein the cells include a steering element and a state change element coupled between the input and output terminals.

57. The array defined by claim 53 wherein the cells have a generally rectangular cross-section.

58. The array defined by claim 53 wherein the cells comprise silicon and silicon dioxide.

59. The array defined by claim 53 wherein the conductors of levels 1, 3... are in vertical alignment with one another.

60. The array defined by claim 53 wherein the conductors in one of the sets of levels 1, 3... and levels 2, 4... are staggered in the vertical direction.

61. The array defined by claim 53 wherein the conductors comprise polysilicon.

62. The array defined by claim 53 wherein the array is fabricated on a silicon substrate.

63. The array defined by claim 62 including a contact extending from one of the conductors in the odd numbered levels 1, 3, ... to the substrate.

64. The array defined by claim 62 including a contact extending from one of the conductors in the even numbered levels 2, 4, ... to the substrate.

65. The array defined by claim 62 including at least one contact extending from the highest level to the substrate.

66. The array defined by claim 62 wherein a contact is made up of several contacts, one for each of the layers.

67. A process for fabricating a memory array comprising:

(a) forming a first layer of conductive material;

(b) forming a plurality of second layers for defining memory cells on the first layer;

(c) patterning the second layers into a plurality of parallel, spaced-apart strips;

(d) etching the first layer in alignment with the strips formed from the second layers;

(e) forming insulating material between the strips of first layer material and the strips formed from the second layers;

(f) forming a third layer of conductive material on the insulating material and the strips formed from the second layer;

(g) forming a plurality of fourth layers for defining memory cells of the second level;

(h) patterning the fourth layers into a plurality of parallel, spaced-apart strips, the strips formed from the fourth layers running generally perpendicular to the strips formed from the first layer;

(i) etching the third layer and the strips formed from the second layers in alignment with the strips formed from the fourth layers.

68. The process defined by claim 67 including forming a fifth layer of conductive material on the strips formed from the fourth layer;

patterning the fifth layer into a plurality of parallel, spaced-apart conductors running generally perpendicular to the strips in the fourth layer; and,

etching the strips formed from the fourth layer in alignment with the conductors thereby defining additional memory cells.

69. The process of claim 67 repeating steps (a) through (i).

70. The process defined by claim 69 with the steps of claim 68.

71. The process defined by claim 67 repeating the steps (a) through (f) a plurality of times.

72. The process defined by claim 71 with the steps of claim 68.

73. The process defined by claim 67 wherein a dielectric is applied and a planarization step occurs after the etching of the first layer and prior to the forming of the third layer.

74. The process defined by claim 73wherein the planarization comprises chemical-mechanical polishing.

75. The process defined by claim 67 including depositing an insulator and etching it back to planarize the structure and opening electrical contacts to the strips formed from the second layer between steps (d) and (e).

76. The process defined by claim 67 wherein the plurality of second layers and plurality of fourth layers each comprise layers of polysilicon and silicon dioxide.

77. The process defined by claim 76 wherein the polysilicon is doped such that each memory cell includes a diode.

78. The process defined by claim 76 wherein the silicon dioxide in each layer forms part of an antifuse.

79. The process defined by claims 67 or 73 wherein a planarization step occurs after the forming of the second layers and before the forming of the third layer.

80. The process defined by claim 79 wherein the planarization is performed by chemical-mechanical polishing.

81. The process defined by claim 79 including forming openings for contacts after the planarization.

82. The process defined by claim 76 wherein the polysilicon is deposited at low temperature using chemical vapor deposition.

83. The process defined by claim 67 including the deposition of a barrier metal layer after the forming of the first layer and prior to the forming of the second layers.

84. The process defined by claim 67 including the deposition of a barrier metal layer after the forming of the third layer and prior to the forming of the fourth layer.

85. The process defined by claim 67 wherein the fabrication includes the fabrication of contacts and where contact openings are made followed by the deposition of silicon into the openings.

86. The process defined by claim 67 including the use of ion implanted silicon.

87. The process defined by claim 67 including the use of in-situ doped silicon.

88. The process defined by claim 87 wherein the silicon is deposited using LPCVD.

89. The process defined by claim 87 wherein the silicon is deposited using PECVD.

90. The process defined by claim 87 wherein the silicon is deposited using PVD.

91. The process defined by claim 87 wherein the silicon is deposited using UHVCVD.

92. A memory comprising:

a monocrystalline silicon substrate with row address decoders and column address decoders and input/output circuitry formed on and in the substrate;

a memory array having a plurality of column conductors and row conductors formed above the substrate and being electrically coupled to the decoders and input/output circuitry;

the array comprising a first plurality of levels each having spaced-apart, parallel, generally coplanar row conductors;

a second plurality of levels interleaved with the first plurality of levels, each having spaced-apart, parallel, generally coplanar column conductors generally perpendicular to the row conductors;

and a plurality of memory cells between each of the levels, each cell being connected to one of the row conductors and one of the column conductors.

93. The memory defined by claim 92 wherein the column decoders and input/output circuitry are folded under the array and coupled to the column conductors.

94. The memory defined by claim 92 wherein the array is divided into a plurality of subarrays.

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